Amendments to the Specification:

Please replace paragraph [0028] of the specification with the following amended paragraph:

[0028] In the liquid crystal display, said gate driver includes a first [[shift]] register sequentially for receiving said first scanning signal and said second scanning signal from said scanning signal supplier; a second [[shift]] register for receiving into an i (i is a natural number) bit of itself the data stored at the i bit of said first [[shift]] register and transmitting to i+1 bit of said first [[shift]] register the data stored at the i bit of itself; a level shifter for receiving the data that contain any one of said first scanning signal and said second scanning signal from said first [[shift]] register, and changing a voltage level suitable for driving said liquid crystal display panel; and an outputter for receiving from said level shifter the data of which the voltage level has been changed and for supplying to said liquid crystal display panel.

Please replace paragraph [0029] of the specification with the following amended paragraph:

[0029] In the liquid crystal display, said scanning signal supplier supplies said second scanning signal to said first [[shift]] register when said first scanning signal is positioned at said second [[shift]] register.

Please replace paragraph [0030] of the specification with the following amended paragraph:

[0030] In the liquid crystal display, said gate driver includes a first [[shift]] register sequentially receiving said first scanning signal and said second scanning signal from said scanning signal supplier; a second [[shift]] register receiving into an i (i is a natural number) bit of itself the data stored at the i bit of said first shift register and transmitting to i+1 bit of said first [[shift]]

register the data stored at the i bit of itself; a level shifter receiving the data that contain any one of said first scanning signal and said second scanning signal from said second [[shift] register, and changing a voltage level suitable for driving said liquid crystal display panel; and an outputter receiving from said level shifter the data of which the voltage level has been changed and supplying to said liquid crystal display panel.

A1

Please replace paragraph [0031] of the specification with the following amended paragraph:

[0031] In the liquid crystal display, said scanning signal supplier supplies said second scanning signal to said first [[shift]] register when said first scanning signal is positioned at said second [[shift]] register.

Please replace paragraph [0049] of the specification with the following amended paragraph:

[0049] Referring to FIG. 7, the gate driver according to the embodiment of the present invention includes a supplier 30 supplying scan data, a first [[shift]] register 32 receiving the scan data from the supplier 30, a second [[shift]] register 38 receiving the scan data from a i^{th} bit of the first shift register 32 and supplying the scan data to a $i+1^{st}$ bit of the first [[shift]] register 32, a level shifter 34 receiving the scan data from the first [[shift]] register 32 and shifting a voltage level suitable for driving the liquid crystal display panel, and an outputter 36 receiving data from the level shifter 34 and supplying to the liquid crystal display panel.

A2

Please replace paragraph [0050] of the specification with the following amended paragraph:

[0050] To describe in detail the motion process of the gate driver, firstly, supplier 30 supplies a scan data corresponding to `1` to a first bit of the first [[shift]] register 32. Then the first [[shift]]

register 32 supplies the provided scan data to a first bit of the level shifter 34 and a first bit of the second [[shift]] register 38.

A2

Please replace paragraph [0052] of the specification with the following amended paragraph:

[0052] Meanwhile, the second [[shift]] register 38 transmits to the second bit of the first [[shift]] register 32 the scan data supplied to the first bit of the second [[shift]] register 38. While having these processes repeated, the gate driver sequentially scans a plurality of gate lines (GL1 to GLm). In the meantime, the supplier 30 supplies the scan data of `1` to the first [[shift]] register 32 when the scan data of `1` is positioned at any bit of the second [[shift]] register 38.

A3

Please replace paragraph [0053] of the specification with the following amended paragraph:

[0053] For example, the supplier 30 supplies the scan data of `1` to the fist bit of the first [[shift]] register 32 when the scan data of `1` is positioned at a third bit of the second [[shift]] register 38. In this way, the gate high volt (Ghv) is supplied to the first gate line (GL1) when the scan data of `1` is supplied to the first bit of the first [[shift]] register 32.

Please replace paragraph [0058] of the specification with the following amended paragraph:

[0058] Meanwhile, the reset data (R) is inputted when the m-10th gate line (GLm-10) being scanned and the actual data (D) is inputted when the m-20th gate line (GLm-20) being scanned in FIG. 8. But, as in FIG. 11, it is possible that the actual data (D) is inputted when the m-10th gate line (GLm-10) being scanned and the reset data (R) is inputted when the m-20th gate line (GLm-20) being scanned. In other words, the scan data of `1` inputted first from the supplier 30 to the first [[shift]] register 32 has a picture data inputted, then the scan data of `1` inputted next from

A4

the supplier 30 to the first [[shift]] register 32 has a black data inputted. In the same manner, the scan data of `1` inputted first from the supplier 30 to the first [[shift]] register 32 has a black data inputted, then the scan data of `1` inputted next from the supplier 30 to the first [[shift]] register 32 has a picture data inputted.

A4

Please replace paragraph **[0059]** of the specification with the following amended paragraph:

[0059] Also, the scan data can be inputted from the supplier 30 to the second [[shift]] register (50), as shown in FIG. 12, in the present invention. At this time, the first [[shift]] register 32 and the second [[shift]] register (50) have the same bit.